OPTi-386WB PC/AT Chipset (82C391/82C392/82C206)

Preliminary

82C391/82C392 DATA BOOK

Version 1.1
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Disclaimer

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Table of Contents

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1. 82C391/82C392 OVERVIEW

1.1 Introduction

The OPTi-386WB is a highly integrated PC/AT VLSI chipset, for the high end 386-based AT systems. It includes System Controller (SYSC,82C391), Data Buffer Controller (DBC,82C392) and Integrated Peripheral Controller (82C206). It is designed for system running from 25 Mhz, 33 Mhz and up to 40 Mhz.

SYSC integrates the write-back cache controller , local DRAM control logic , AT bus and CPU interface circuitry DBC includes the data buffers, AT bus control, decoding logic for keyboard controller, reset and clock generation logic.

A high performance 386-based system can be implemented easily with 386 WB PC/AT chipset.

1.2 Features

* Two 160-pin CMOS Plastic Flat Package (PFP), and one 84-pin PLCC
* Copy-Back Direct Mapped Cache with size of 32 KB, 64 KB, 128 KB and 256 KB
* 16 Bytes Line Size
* Optional 0/1 Wait State for Cache Write Hit
* On-chip Comparator for Hit or Miss decision
* Support 256K/1M/4M DRAM
* Up to 64 MB Local High Speed Page Mode DRAM memory space
* Burst Line Fill during Cache Read Miss
* Two Non-Cacheable Regions Control
* Option for Cacheable video BIOS
* Shadow RAM support
* Hidden Refresh
* Slow Refresh Support for Laptop Application.
* 8042 Emulation for Fast CPU Reset and GateA20 generation
* Turbo/Slow speed operation
* AT bus clock = CLK2IN/8 or CLK2IN/6
* 0 or 1 wait state for 16-bit AT bus cycle
* CAS# before RAS# refresh to reduce power comsumption

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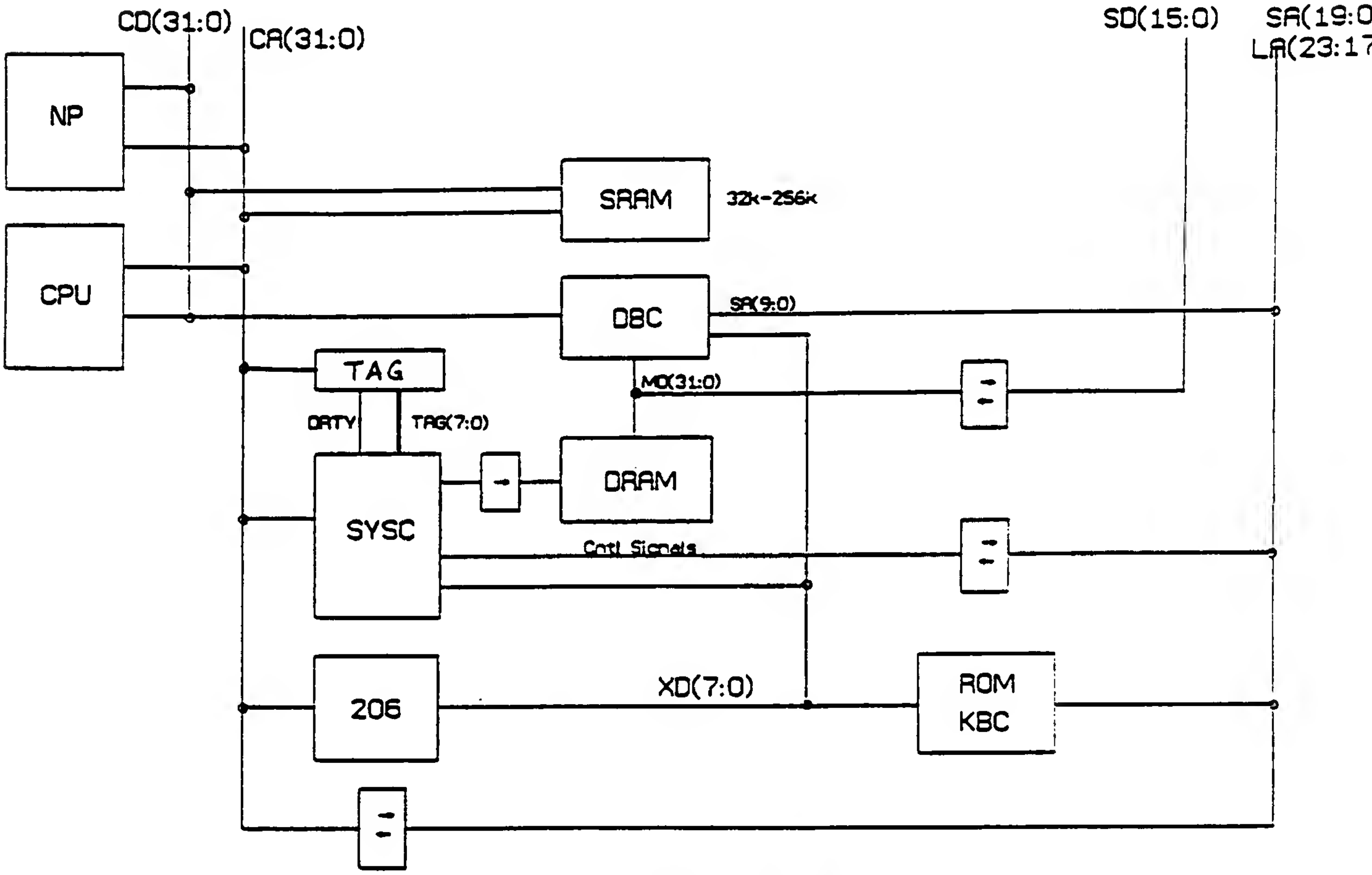
1.3 SYSTEM BLOCK DIAGRAM

Figure 1. shows system address and data bus block diagram of 386WB-based system.



BLOCK DIAGRAM

2. 82C391 SYSTEM CONTROLLER (SYSC)

2.0 Features:

- Reset Control for CPU and Numeric Processor.
- Clock Generation for CPU, Processor and AT-BUS
- CPU Interface Control.
- Integrated Write-back Cache Controller with Built-in Tag Comparator.
- Page Mode DRAM Controller
- Burst Line Fill Control Logic
- Two Noncacheable Address Comparators
- Decoupling Refresh for Local DRAM and AT-Bus Memory
- 2 DMA upper address latches.

2.1 Reset Logic

SYSC monitors two reset sources, RST1# and RST2#, and generates CPURST and NPRST signals to CPU and coprocessor, respectively.

RST1# from DBC is the cold reset which is originated from either Power Good signal of power supply or the reset switch. When RST1# is asserted low, SYSC activates CPURST and NPRST to reset the CPU and numeric coprocessor simultaneously. RST2# is generated when a "warm reset " from 8042 (or 8742) keyboard controller is required. RST2# can be connected to either keyboard controller or DBC. DBC emulates the RST2# generation sequence and provides a faster reset to SYSC. The warm reset only activates CPURST.

CPURST also can be activated by programming bit 0 of indexed register 20h from 0 to 1, then executing a "HALT" instruction.

2.2 System Clock Generation

SYSC has two high frequency clock inputs, OSCIN and CLK2IN. The CLK2IN is the clock source of SYSC's internal state machine while OSCIN, which comes directly from a buffered oscillator, is used to generate CPURST.

ATCLK can be derived from CLK2IN/6 or CLK2IN/8 depending ton the state of "BCLKS" input pin. BCLKS must be pulled to either a high or low state through a 2- position jumper. If BCLKS is tied to low, CLK2IN/8 is selected, otherwise CLK2IN/6 is chosen.

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2.3 Cache Interface

The 82C391 cache controller monitors the status of internal HIT# and NCA# signal to determine whether the current cycle is a cache-hit or cache-missed. During the cache read miss cycle and DIRTY bit is not active, the cache controller asserts TAGWE# to update the TAG RAMs, CAWE# is also activated to update the cache memory. If DIRTY bit is active, the whole cache line of 16 bytes will first be written back into DRAM, then 16 bytes DRAM data addressed burst into cache memory.

When cache write hit happens, the data are written into cache memory and Dirty bit is set. Data will be written into DRAM directly if write-miss cycle occurs.

2.4 Cache Control Subsystem

The Tag comparator is built inside SYSC to generate the HIT# signal internally.This approach improves the system speed as well as reduces the board real estate.

In order to simply the design without increasing cost or degrading system performance, the SYSC has been designed to operate at non-pipeline mode and support line size of 16 bytes.

The following table shows the cache sizes supported, tag RAM used, cacheable main memory size, and addresses for the tag and cache memory fields.

Cache Size (Kb)	Tag Field Address/ Tag RAM size	Cache RAM Address /Cache RAMs	Cachable Main Memory(Mb)
32	A22 - A15 2KX9	A14 -A4 4 8KX8	8
64	A23 -A16 4KX9	A15 -A4 8 8KX8	16
128	A24 - A17 8KX9	A16 - A4 4 32KX8	32
256	A25 - A18 16KX9	A17 -A4 8 32KX8	64

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2.5 Local DRAM Control Subsystem

SYSC supports up to 4 bank, page mode local memory. DRAM devices can be 256K, 1M or 4M and total memory can be up to 64 Mb. The following table illustrates the configurations supported.

Bank 0	Bank 1	Bank 2	Bank 3	Total
256k	x	x	x	1M
256k	256k	x	x	2M
1M	x	x	x	4M
256k	1M	x	x	5M
1M	1M	x	x	8M
1M	1M	1M	x	12M
1M	1M	1M	1M	16M
4M	x	x	x	16M
1M	4M	x	x	20M
4M	1M	x	X	20M
1M	1M	4M	x	24M
1M	4M	1M	x	24M
4M	1M	1M	x	24M
1M	1M	4M	1M	28M
1M	4M	1M	1M	28M
4M	1M	1M	1M	28M
4M	4M	x	x	32M
1M	4M	4M	x	36M
4M	1M	4M	x	36M
4M	4M	1M	x	36M
1M	1M	4M	4M	40M
1M	4M	4M	1M	40M
4M	1M	4M	1M	40M
4M	4M	1M	1M	40M
4M	4M	4M	x	48M
1M	4M	4M	4M	52M
4M	1M	4M	4M	52M
4M	4M	4M	1M	52M
4M	4M	4M	4M	64M

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2.6 Shadow RAM

The access time to local DRAM is much faster than that of EPROM, SYSC provides shadow RAM capability to speed up the BIOS,video BIOS and other adaptor BIOS accessing. The BIOS can be copied into corresponding RAM address spaces and write-protected. After the copy process, every access to the address space of the BIOS will instead be directed to DRAM and the system performance is highly enhanced.

Shadow RAM address starts from C0000h-FFFFFh. Address range C0000h-EFFFFh are enabled in 16KB memory chuck where system BIOS F0000h-FFFFFh is in 64 KB.

The access scheme of system BIOS (F0000h-FFFFFh) area is defaulted to read from EPROM and write into corresponding DRAM address range. If bit 7 of index register 22h is enabled, the source of read is changed from EPROM to DRAM and DRAM is write-protected.

2.7 AT Bus State Machine

AT state machine monitors status signals, M16#, IO16#, Chrdy and Nows# from AT bus and generates the command, bus conversion, and control signals to AT bus. It also respond to AT bus master and DMA controller to control proper data and address buffers directions.

2.8 Bus Arbitration Logic

Arbitration between CPU, DMA/master and Refresh request is implemented inside SYSC. For DMA and bus master cycles, SYSC generates HRQ to CPU and CPU will respond by asserting HLDA and release the bus controls to the requesting devices. When refresh happens and the hidden refresh function is enabled, no HRQ signal is generated, and the CPU will continue its current program execution if the code and data are resided in the cache memory and hence the system performance is boosted. The arbitration is based on first-come, first serve basis.

2.9 Refresn Logic

The SYSC supports both normal refresh and hidden refresh. The average refresh period can be 16Us or 64 Us, depending on whether the slow refresh is disabled or not. Normal refresh is conventional where the hidden refresh separate DRAM and AT-bus memory refresh process. Once the hidden refresh is turned on, the AT-bus controller will perform arbitration among the CPU AT cycle, DMA cycle, and refresh cycle. The DRAM controller will perform the arbitration between CPU DRAM and refresh cycle.

During AT-bus refresh cycle, the refresh address is generated by the DBC.

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2.10 System BIOS ROM and I/O Ports

The SYSC supports both 8 bit and 16 bit EPROM cycle. If 8 bit EPROM is selected, the system BIOS EPROM will reside on XD bus. If 16 bit EPROM is required, the BIOS EPROM must be seated in SD bus and ROMCS# should be connected to M16# through a open collecter to tell the SYSC that the current system BIOS is a 16 bit I/O cycle.

The direction of XD-bus data buffer is normally driven toward XD bus. XD-bus buffer will drive toward local data bus when I/O read cycle with address smaller than F0h or 8-bit BIOS ROM cycle.

2.11 Turbo Switch

The system is operating at the full speed if the TURBO pin is asserted high. When TURBO pin is sensed low, SYSC will hold two third of the CPU time to slow down the system execution speed. The source of non-Turbo hold request is OUT1 input from 82C206. The frequency of hold request is one third of that of OUT1 input pin. This non-Turbo hold request only hold the CPU and does nothing else. It is arbitrated between HRQ and normal refresh request.

2.12 Flexible Multiplexed DRAM Address

The following table describes how the DRAM address lines are multiplexed when different memory de`vices types are used.

Address to MA bus Mapping

Mem addr	256K Row	256K Col	1M Row	1M Col	4M Row	4M Col
MA0	A2	A12	A2	A12	A2	A12
MA1	A3	A13	A3	A13	A3	A13
MA2	A4	A14	A4	A14	A4	A14
MA3	A5	A15	A5	A15	A5	A15
MA4	A6	A16	A6	A16	A6	A16
MA5	A7	A17	A7	A17	A7	A17
MA6	A8	A18	A8	A18	A8	A18
MA7	A9	A19	A9	A19	A9	A19
MA8	A10	A11	A10	A20	A10	A20
MA9	X	X	A11	A21	A11	A21
MA10	X	X	X	X	A12	A22

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3. SYSC SIGNALS DESCRIPTIONS

3.1 Clock and Reset

Name	Type	Pin No	Description
OSCIN	I	82	Crystal oscillator Input which has a frequency equal to twice the rated CPU clock. This signal is used to generate CPURST.
CLK2I	I	79	Clk2 input for SYSC internal state machine.
BCLKS	I	14	BCLK Selection. Low BCLK = OSCIN/8. High BCLK = OSCIN/6.
BCLK	O	83	BCLK to AT bus.
RST1#	I	138	Cold reset input either from Powergood signal of power supply or from Reset Switch
RST2#	I	113	CPU Reset input from Keyboard Controller or from DBC's ERST2# pin.
CPURST	O	90	Reset for 386 processor.

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3.2 CPU Interface

Name	Type	Pin No	Description
CA(31:24)	I	68-65,33-30	CPU Address Lines 31-24. Input only
CA(23:17)	I	64-58	CPU Address Lines 23-17. Input only
CA(16:8)	B	57-51,49-48	CPU Address Lines 16-8. These are input pins during CPU cycle. CA(16:9) are output pins for DMA address A16-A9 by latching XD(7:0) during 16-bit DMA cycle and CA(15:8) are DMA address A15-A8 for 8-bit DMA cycle.
CA(7:2)	I	47-42	CPU Address Lines 7-2. Input only.
BE(3:0)	B	29-26	Byte Enable 3-0. These are inputs during CPU cycle and are outputs during DMA and master cycle, which derived from XA0, XA1 and SBHE# from AT bus.
ADS#	I	88	Status input from CPU. This active low signal indicates the CPU is starting a new cycle.
WR#	I	85	CPU Write or Read Cycle Status. It indicates a write cycle if high and read cycle if low.
DC#	I	86	CPU Data or Code Cycle Status. It indicates data transfer operations when high, or control operations(code fetch, halt, etc.) when low.
MIO#	I	84	CPU Memory or I/O Cycle Status. It indicates a memory cycle if high, and I/O cycle if low.
LDEV#	I	133	Indication of CPU local Bus device Cycle, i.e. Weitek 3167 coprocessor. This signal is sampled at the end of 1st T2.
RDY#	O	89	Ready output for CPU to terminate the current cycle.This pin is not a tri-state output.
RDYI#	I	132	Local Device Ready Input, It will be synchronized by SYSC before sending to CPU.
TURBO	I	13	Turbo Mode Selection. I f Turbo# pin is tied to high; the system runs at full speed, otherwise, the SYSC will hold two third of the CPU time.

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3.3 Numeric Processor Interface

Name	Type	Pin No	Description
NPERR#	I	91	Numeric Processor Error Indication.
NPRST	O	92	Numerical Processor Reset. CPURST or I/O write to port F1h will assert NPRST. It is asserted for 40 clk2 and 80387 can not be accessed within 50 clk2 after NPRST is negated.
BSYTOG#	O	115	Toggled BUSY# when 80387 is not installed.

3.4 External Cache Control

Name	Type	Pin No	Descriptions
TAG(7:0)	I	77-71,69	TAG RAM Output Lines 7-0.
DRTY	B	34	Dirty Bit of Tag RAM to indicate its line has been written into.
TAGWE#	O	39	TAG RAM Write Enable. It is used to update the tag RAM.
CAEOE#	O	22	External Cache Even Bank Output Enable; It is always activated for 32k and 128k cache memory. CAEOE# is also asserted when CA15 and CA17 are low for 64KB and 256 KB cache memory, respectively.
CAOOE#	O	23	External Cache Odd Bank Output Enable. It is deactivated for 32 KB and 128 KB cache. CAOOE# is only asserted when CA15 and CA17 are high for 64 KB and 256 KB cache memory respectively.
CAEWE#	O	24	External Cache Even Bank Write Enable. It is always activated for 32k and 128k cache size and only asserted when CA15 is low for 64 KB and CA17 is low for 256 KB cache respectively.
CAOWE#	O	25	External Cache Odd Bank Write Enable. It is only asserted when CA15 and CA17 is high for 64KB and 256Kb cache respectively.
DRTYW#	O	38	Write strobe to Dirty Bit iof Tag Ram
A3CON	O	37	Cache Address Bit 3 Toggle Control. It is toggled during cache read miss cycle.
A2CON	O	36	Cache Address Bit 2 Toggle Control; It is toggled during cache read miss cycle.

3.5 Local DRAM Interface

Name	Type	Pin No	Description
DWE#	O	131	DRAM Write Enable signal.
RAS(3:0)#	O	12-9	DRAM Row Address Strobe.
CAS(15:0)#	O	8-2,159-151	DRAM Column Address Strobe.
MA(10:0)	O	149-139	DRAM Row/Column Address Line 10-0.

3.6 DBC Interface

Name	Type	Pin No	Description
LMEN#	O	119	Local Memory Acessed Indication.Used by DBC to control the bus flow.
DLE	O	118	DRAM Read Data Latch Enable; used for parity checking.
MIO16#	O	114	Latched AT-bus 16-bit Slave Status; used for bus conversion.
PCKEN#	O	117	Parity Checking Enable; used by DBC to perform parity checking.
ATCYC#	O	116	AT Cycle Indication for CPU cycle.

3.7 Bus Arbitration

Name	Type	Pin NO	Description
HRQ	I	18	DMA or Master Cycle Request from 82C206
OUT1	I	111	Refresh Request from Timer1 Output.
HLDA	I	78	CPU Hold Acknowledge.
ADS8	O	110	8-bit DMA Transfer Address Strobe. The SYSC has to latch XD(7:0) by using ADS8 and translate to CA(15:8) outputs.
AEN8#	O	16	8-bit DMA Cycle Indication.
ADS16	O	109	16-bit DMA Transfer Address Strobe. The SYSC has to latch XD(7:0) by using ADS16 and translate to CA(16:9) outputs.
AEN16#	O	17	16-bit DMA Transfer Indication.
HOLD	O	35	HOLD Request to CPU. Hidden refresh will not hold the CPU.
HLDA1	O	108	DMA or Master Cycle Granted Notice.
RFSH#	B	95	AT Refresh Cycle Indication. It is an intput pin during master or DMA cycle.

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3.8 AT-BUS Interface

Name	Type	Pin No	Description
CA0	B	104	System Address Line 0, it is an input pin during master or 8-bit DMA cycle; becomes output pin during CPU, 16-bit DMA cycle or refresh cycle.
CA1	B	105	System Address Line 1, it is an input pin during master or DMA cycle; becomes output pin during CPU or refresh cycle.
CHRDY	I	136	Channel Ready Input from AT-BUS. It is a schmit trigger input pin.
NOWS#	I	137	Zero Wait State Input from AT-BUS. It is a schmit trigger input pin. Note that the system BIOS ROM is treated as AT zero wait state cycle.
IO16#	I	135	16-bit IO Slave Cycle Status. It is a schmit trigger input pin.
M16#	I	134	16-bit Memory Slave Cycle Status; it is a schmitt trigger input pin.
GATEA20	I	112	Gate A20 Input from 8042 or DBC emulated gateA20 pin.
GA20	B	87	Gated AT bus A20; connected to AT bus LA20 indirectly through a buffer. It's a input pin during master cycle. The GA20 should not be gated with GATEA20 or fast GATEA20 during DMA cycle.
XD(7:0)	B	129-122	Peripheral Data Bus Line 7-0.Two purposes for these pins: program the internal index register.* latch the DMA high order address.
IORD#	B	94	AT IO Read Command. It is an input pin during DMA or master cycle.
IOWR#	B	93	AT IO Write Command. It is an input pin during DMA or master cycle.
MRD#	B	97	AT Memory Read Command. It is an input pin during DMA or master cycle.
MWR#	B	103	AT Memory Write Command. It is an input pin during DMA or master cycle.
SMRD#	O	98	AT Memory Read Command, for address below 1 mega. It has to be activated during refresh cycle.
SMWR#	O	102	AT Memory Write Command, for address below 1 MB memory space.
ALE	TO	96	AT Bus Address Latch Enable to represent that the AT cycle has started. It is tristated during non-CPU cyle.

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Name	Type	pin No	Description
SBHE#	O	106	AT Bus High Enable. It is an input pin during master cycle.
INTA	O	107	Interrupt Acknowledge Cycle Indication. Hold will not send to CPU between the INTA* cycles.
ROMCS#	O	15	System BIOS ROM Output Enable. System BIOS ROM accessing could be either 8-bit or 16-bit. This signal will be asserted from the end of the first T2 to the end of the last T2.

3.9 Ground and VCC

Name	Type	Pin No	Description
VCC	I	1,20,40,81,100,120	+5V
GND	I	19,21,41,50,70,80,99,101,121,130,150,160	VSS or Ground

4. SYSC REGISTERS DESCRIPTIONS

There are twelve configuration registers inside the 82C391. An indexing scheme is used to access all the registers of OPTi-386WB chipset. Port 22h contains the address of the index register and port 24h is used as the data register. Every access to port 24h must be preceded by a write to port 22h even if the same register is being accessed again. All reserved bits are set to zero by default and must be set to zero for future compatibility purpose.

Control Register 1
Index: 20h

BIT	FUNCTION	FAULT
7-6	Revision of 82C391 and is read-only.	0 0
3	Single ALE Enable- SYSC will activate single ALE instead of multiple ALEs during bus conversion cycle if this bit is enabled. 0 =disable 1 =enable	0
2	Extra AT Cycle Wait State Enable. Insert one extra wait state in standard AT bus cycle. 0 = disable 1 =enable	0
1	Keyboard and Fast Reset Control - turn on this bit requires "Halt" instruction to be executed before SYSC generates CPURST. .from keyboard reset 0 =disable 1= enable	0
0	Fast Reset Enable- alternative fast CPU reset. 0 = disable 1 =enable	0

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Control Register 2
Index: 21h

BIT	FUNCTION	DEFAULT
7	Master Mode Byte Swap Enable 0 = disable 1 = enable	0
6	Fast Keyboard Reset Delay Control 0 = Generate reset pulse 2 us later 1 = Generate reset pulse immediately	0
5	Parity Check 0 = enable 1 =disable	0
4	Cache Enable 0 = disable 1 = enable	0.
3-2	Cache Size <u>3 2 Cache Size</u> 0 0 32KB 0 1 64KB 1 0 128KB 1 1 256KB	00
1-0	Cache Write Control <u>1 0 Write Control</u> 0 0 = 1 Wait state, write hit cycle 0 1 = 0 Wait state for 32KX8 SRAMs(128K or 256K cache) 1 0 = Not used 1 1 = 0 Wait state for 8KX8 SRAMs(32K or 64 K cache)	00

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Shadow RAM Control Register I
Index: 22h

BIT	FUNCTION	DEFAULT
7	ROM Enable 1 = read from ROM, write to DRAM. 0 = read/write on RAM and DRAM is write-protected	1
6	Shadow RAM at D0000h - DFFFFh Area 0 = Disable 1 = Enable	0
5	Shadow RAM at E0000h - EFFFFh Area 0 = Disable 1 = Enable	0
4	Shadow RAM at D0000h - DFFFFh Area Write Protect Enable 0 = Disable 1 = Enable	0
3	Shadow RAM at E0000h - EFFFFh Area Write Protect Enable 0 = Disable 1 = Enable	0
2	Hidden Refresh- refresh enable (without holding CPU) 1 = Disable 0 = Enable	1
1	Unused Bit	0
0	Slow Refresh Enable (4 times slower than the normal refresh) 0 = Disable 1 = Enable	0

Shadow RAM Control Register II
Index: 23h

BIT	FUNCTION	DEFAULT
7	Shadow RAM at EC000h-EFFFFh area 0 = Disable 1 = Enable	0
6	Shadow RAM at E8000h-EBFFFh area 0 = Disable 1 = Enable	0.
5	Shadow RAM at E4000h-E7FFFh area 0 = Disable 1 = Enable	0.
4	Shadow RAM at E0000h-E3FFFh area 0 = Disable 1 = Enable	0.
3	Shadow RAM at DC000h-DFFFFh area 0 = Disable 1 = Enable	0
2	Shadow RAM at D8000h-DBFFFh area 0 = Disable 1 = Enable	0.
1	Shadow RAM at D4000h-D7FFFh area 0 = Disable 1 = Enable	0.
0	Shadow RAM at D0000h-D3FFFh area 0 = Disable 1 = Enable	0.

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DRAM Control Register I
Index: 24h

BIT	FUNCTION	DEFAULT
7	2 Bank Mode. When enabled, only first two banks(Bank 0 and Bank 1) are used. 1 = Disable 0 =Enable	0
6-4	DRAM types used for bank0 and bank1. See the following table	000
3	Not used	0
2-0	DRAM types used for bank 2 and bank 3. See the following table. Bit 2-0 are not used when bit 7 is set to "0".	111

Bits 7 6 5 4	Bank 0	Bank 1
1 0 0 0	1M	X
1 0 0 1	1M	1M
1 0 1 0	1M	4M
1 0 1 1	4M	1M
1 1 0 0	4M	X
1 1 0 1	4M	4M
1 1 1 X	X	X
0 0 0 0	256K	X
0 0 0 1	256K	256K
0 0 1 0	256K	1M

Bits 7 2 1 0	Bank 2	Bank 3
1 0 0 0	1M	X
1 0 0 1	1M	1M
1 0 1 0	X	X
1 0 1 1	4M	1M
1 1 0 0	4M	X
1 1 0 1	4M	4M
1 1 1 X	X	X

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DRAM Control Register II
Index: 25h

BIT	FUNCTION	DEFAULT
7-6	Read cycle wait state 7 6 Additional wait States 0 0 Not used 0 1 0 1 0 1 1 1 2 Note: Base wait states is "3".	11
5-3	Write cycle wait state 5 4 3 Additional wait states 0 0 0 0 0 1 0 1 1 0 0 2 1 1 0 3 0 0 1 not used Note: Base wait states is "2".	110
2-0	unused	00

Shadow RAM Control Register III
Index: 26h

BIT	FUNCTION	DEFAULT
6	Shadow RAM copy enable for address area C0000h-EFFFFh 0 = Read/write at AT bus 1 = Read from AT bus and write into shadow RAM	0
5	Shadow write protect at address area C0000h-EFFFFh 0 = Write protect disable . 1 = Write protect enable	1
4	Shadow RAM enable at C0000h- CFFFFh area 0 = Enable 1 = Disable	1
3	Enable shadow RAM at CC000h-CFFFF area 0 = Disable 1 = Enable	0
2	Enable shadow RAM at C8000h-C8FFF area 0 = disable 1 = Enable	0
1	Enable shadow RAM at C4000h-C7FFFh area 0 = Disable 1 = Enable	0
0	Enable shadow RAM at C0000h-C3FFFh area 0 = Disable 1 = Enable	0

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Control Register 3
Index: 27h

BIT	FUNCTION	DEFAULT
7	Enable NCA# pin to low state, 0=Disable 1 =Enable	1
6-5	Unused	00
4	Video BIOS at C0000h-C8000h area non-cacheable 0 = Cacheable 1 = Non-cacheable	1
3-0	Cacheable address range for local memory, see following table	0001

Note. Memory area at 640K-1M is defaulted to be non-cacheable.

Bits 3 2 1 0	Cachable Address range
0 0 0 0	0 - 64 Mb
0 0 0 1	0 - 4 Mb
0 0 1 0	0 - 8 Mb
0 0 1 1	0 - 12 Mb
0 1 0 0	0 - 16 Mb
0 1 0 1	0 - 20 Mb
0 1 1 0	0 - 24 Mb
0 1 1 1	0 - 28 Mb
1 0 0 0	0 - 32 Mb
1 0 0 1	0 - 36 Mb
1 0 1 0	0 - 40 Mb
1 0 1 1	0 - 44 Mb
1 1 0 0	0 - 48 Mb
1 1 0 1	0 - 52 Mb
1 1 1 0	0 - 56 Mb
1 1 1 1	0 - 60 Mb

Note:

1. 1 bank of 256K DRAM - Cacheable address range is defaulted to 0 - 1 Mb
2. 2 banks of 256K DRAM - Cacheable address range is defaulted to 0 -2 Mb.
3. 1 bank of 256K and 1M DRAM -Cacheable address range must be set to 0 - 4 Mb.

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Non-cachable Block 1 Register I-
Index: 28h

This register is used in conjunction with Index 29h register to define a non-cacheable block. The starting address for the Non-Cacheable Block must have the same granularity as the block size. For example, if a 512 Kb non-cacheable block is selected, its starting address is a multiple of 512 Kb; consequently, only address bits of A19-A23 are significant, A16-A18 are "don't care".

BIT	FUNCTION	DEFAULT
7-5	Size of non-cachable memory block 1, See following table	100
4-2	Unused	000
1-0	Address bits of A25 and A24 of non-cachable memory block 1	00

7 6 5	Block Size
0 0 0	64K
0 0 1	128K
0 1 0	256K
0 1 1	512K
1 x x	Disabled

Non-cachable Block 1 Register II
Index: 29h

BIT	FUNCTION	Default
7-0	Address bit A23-A16 of non-cachable memory block 1	0001xxxx

	Valid Starting Address Bits							
Block Size	A23	A22	A21	A20	A19	A18	A17	A16
64K	V	V	V	V	V	V	V	V
128K	V	V	V	V	V	V	V	x
256K	V	V	V	V	V	V	x	x
512K	V	V	V	V	V	x	x	x

x = Don't Care
V = Valid Bit

Non-cachable Block 2 Register I
Index: 2Ah

This register is used in conjunction with Index 2Bh register to define a non-cacheable block. The starting address for the Non-Cacheable Block must have the same granularity as the block size. For example, if a 512 Kb non-cacheable block is selected, its starting address is a multiple of 512 Kb; consequently, only address bits of A19-A23 are significant, A16-A18 are "don't care".

BIT	FUNCTION	DEFAULT
7-5	Size of non-cacheable memory block 1, See following table	100
4-2	Unused	000
1-0	Address bits of A25 and A24 of non-cachable memory block 1	00

7 6 5	Block Size
0 0 0	64K
0 0 1	128K
0 1 0	256K
0 1 1	512K
1 x x	Disabled

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Non-cachable Block 1 Register II
Index: 2Bh

BIT	FUNCTION	Default
7-0	Address bit A23-A16 of non-cachable memory block 1	0001xxxx

	Valid Starting Address Bits							
Block Size	A23	A22	A21	A20	A19	A18	A17	A16
64K	V	V	V	V	V	V	V	V
128K	V	V	V	V	V	V	V	x
256K	V	V	V	V	V	V	x	x
512K	V	V	V	V	V	x	x	x

x = Don't Care
V = Valid Bit

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5. 82C392 DATA BUFFER CONTROLLER(DBC)

DBC is a 160 pin PFP (Plastic Flat Package) device. It includes the following functions:

* Data Bus Conversion
* Parity Generation/Detection
* AT-BUS direction control
* Reset logic
* Clock source for 206 and 8042
* Chip select for Keyboard Controller and RTC
* Speaker Control
* Port B, 70H and NMI Logic
* Numerical Processor Interface
* Keyboard reset and Gate A20 emulation logic

Some functions mentioned above will be described in the following paragraphs.

5.1 Data Bus Conversion

The DBC performs data bus conversion when CPU accesses to 16 or 8 bit devices through 32/16 bit instructions. The bus conversion is also supported for DMA/Master cycle for the transfer between local DRAM or cache memory and devices which resides on AT Bus. During the process, DBC provides all the signals necessary to control the external bi-directional data buffers.

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5.2 Parity Generation/Detection Logic

For local DRAM write cycle, DBC generates a parity bit for each byte of write data from the processor. These parity bits are stored into the parity bits of the local DRAM. When a local memory read cycle occurs, the data bytes, together with the parity bits, will be fed into DBC. Parity generation/detection logic will compare the parity bit and the parity generated from the data byte. If a mismatch happens, the parity error will be generated. The parity checking time is the timing window of "PCKEN" signal.

5.3 Clock Generation and Reset Control

In order to reduce the components count, DBC provides the clock sources for the timer 1 of 80C206 and 8042 keyboard controller. The clocks are derived from 14.3 Mhz. The Clock frequency for 80C206 is 1.19 Mhz , 14.3Mhz divided by 12, while the one for 8042 is 7.15 Mhz, 14.3Mhz divided by 2.

The DBC also monitors both the PWGD# (Powergood) signal from power supply and Reset signal from the reset switch. The reset signal, RST1, is then directed to SYSC to generate the "cold reset".

SYSC can accept the "warm reset RST2" from either the keyboard controller or DBC both of which emulates the keyboard controller warm reset sequence and generate at a much faster speed. The choice is the user decision.

5.4 Numeric Coprocessor Interface

The DBC provides the numeric coprocessor supports for 387 and 3167 without external logic components.

DBC samples NPERR# during power on reset. A low indicates an 80387 is present, and the coprocessor cycle will be terminated by a Ready# signal from 80387. NPBSY# indicates a coprocessor instruction is currently being executed and this signal is relayed to CPU via BUSY# signal line. . If BUSY# is active and a numeric coprocessor error NPERR* occurs, the NPBUSY# will be latched and INT13 is generated. Another source of INT13 come from the WINT# from the Weitek 3167 coprocessor. Latched BUSY# and INT13 can be cleared by a I/O port F0H write command.

6. 82C392(DBC) PIN DESCRIPTIONS

6.1 Clock and Reset

Name	Type	Pin No	Description
OSCX1	I	43	14.3 Mhz osc. input.
OSCX2	O	42	14.3 Mhz osc. output.
OSC	O	82	14.3 Mhz osc. Output to AT bus.
OSC12	O	83	1.19 Mhz output to 206
OSC2	O	85	14.3 Mhz/2 output for 8042 clock.
OSC2#	O	84	14.3 Mhz/2 inverted output for 8042 clock.
PWGD#	I	16	Power Good Status from power supply. It is buffered through a Schmitt- trigger gate.
RSTSW	I	4	Reset Switch Input.. It is buffered through a Schmitt-trigger gate.
RST1#	O	10	Power-up or cold Reset signal derived from PWGD# or RSTSW.

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6.2 Address and Data Buses

Name	Type	Pin No	Description
D(31:23)	B	79-71	CPU Data Bus
D(22:14)	B	69-61	CPU Data Bus
D(13:5)	B	59-51	CPU Data Bus
D(4:0)	B	49-45	CPU Data Bus
A(9:0)	I	119-110	Buffered AT SA (9:0) address lines.
SBHE#	I	25	Byte High Enable from AT bus and SYSC.
BE(3:0)#	I	39-36	CPU Byte Enables; used for data bus parity checking of valid byte.
MD(31:26)	B	156-151	Local DRAM Data Bus.
MD(25:17)	B	149-141	Local DRAM Data Bus
MD(16:8)	B	139-131	Local DRAM Data Bus
MD(7:0)	B	129-122	Local DRAM Data Bus
MP(3:0)	B	2,159-157	Local DRAM data bus Parity Bits.
XD(7:4)	B	104-101	XD Data Lines 7-4.
XD(3:0)	B	99-96	XD Data Lines 3-0.

6.3 Bus Arbitration

Name	Type	Pin No	Description
HLDA	I	32	Hold Acknowledge from CPU in response to hold request.
AEN8#	I	28	8-bit DMA Cycle Indication.
AEN16#	I	27	16-bit DMA Cycle Indication.
AEN#	O	106	DMA Cycle Indication.
MASTER#	I	26	Master Cycle Indication.
RFSH#	I	24	Refresh Cycle Indication.

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6.4 SYSC Interface

Name	Type	Pin No	Description
INTA#	I	23	Interrupt Acknowledge, used to direct the data flow.
ROMCS#	I	22	System BIOS ROM Chip Select,, used to direct the data bus flow.
LMEN#	I	21	Local Memory Enable. Indicate the current cycle is local DRAM Access. It is used to control the bus direction.
WR#	I	31	CPU Write or Read Cycle Indication.
DLE	I	17	DRAM Read Data Latch, used to latch the data for parity checking.
DWE#	I	3	DRAM Write Enable, used to enable the write to DRAM.
ATCYC#	I	15	AT Cycle Indication. If asserted, the current access is AT bus cycle.
PCKEN#	I	18	Parity Checking Enable, to enable the Parity error signal if any.
MIO16	I	30	16-bit slave devices access indication. It is used to control the data flow path.
IOWR#	I	11	AT bus I/O Write Command.
IORD#	I	12	AT bus I/O Read Command.
MEMRD#	I	14	AT bus Memory Read Command.
MEMWR#	I	13	AT bus Memory Write Command.

6.5 Numeric Processor Interfaces

Name	Type	Pin No	Description
NPERR#	I	87	Numeric Processor Error from 80387. It is an active low input indicating that an unmasked error happens.
NPBUSY#	I	88	Numeric Processor Busy from 80387 to indicate a coprocessor instruction is under execution.
NPRST	O	89	Reset Numeric Processer
BUSY#	O	34	Latched Coprocessor Busy Output to 80386 to indicate a NPBUSY# or NPERR# signals has occurred.
BSYTOG#	I	9	Busy Toggled Control; used to toggle the BUSY# signal when 80387 coprocessor is not installed.

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Name	Type	Pin No	Description
INT13	O	91	Numeric Processor Interrupt; is an active high output. It is an interrupt request from numeric coprocessor and connected to IRQ13 of interrupt controller.
ERR#	O	33	Error signal to 80386. It reflect the NPERR# signal during the period from RST4# active to first ROMCS#.
WINT	I	92	Weitek 3167 Co-processor Interrupt Request.
PREQI	I	90	80387 coprocessor Request Input.
PREQO	O	35	Numeric Processor Request to 80386.

6.6 Miscellaneous Signals

Name	Type	Pin No	Description
KBDCS#	O	105	Keyboard Controller Chip Select.
NMI	O	95	Non-maskable Interrupt; due to parity error from local memory or AT bus channel check.
SPKD	O	8	Speaker Data Output, derived from the function of OUT2 and port 61H bit1.
GATE2	O	93	Timer 2 Gate Control.
ASRTC	O	94	Real Time Clock Address Strobe.
CHCK#	I	29	AT-BUS Channel Check.
OUT2	O	44	Timer 2 output.
FAST	I	5	FAST is an active high input which will enable the emulation of Fast GATEA20 and Reset Control Enable.
EGTA20	O	7	GateA20 output . It is generated by emulating Keyboard GATEA20.
ERST2#	O	6	RST2# output. It is generated by emulating keyboard RST2#.
M16#	O	19	Master Access Local DRAM invalidation.
SDEN#	O	107	MD-bus to SD-bus Buffer Enable Signal.
SDIR1#	O	109	MD(7:0) to SD(7:0) Buffer Direction Control.
SDIR2#	O	108	MD(15:8) to SD(15:8) Buffer Direction Control.

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6.7 Ground and VCC

Name	Type	Pin No	Description
VCC	I	20,40,86,100,140	+5V
GND	I	1,40,41,50,70,80,81,120,121,130,150,160	VSS or Ground

7. 82C392(DBC) REGISTERS DESCRIPTIONS

Control Register Index 21h(write only)

Bit 7-4 is a duplication of control register index 21h of 82C391.
Bit 3-0 are not used.

I/O Port 60h

Port 60h and 64h are used to emulate the registers of keyboard controller for the generation of a fast Gatea20 signal. The sequence is BIOS transparent, and there is no need for the modification of the current BIOS. The fast gatea20 generation is enabled only when "Fast" is asserted high. The sequence is: first write data "D1h" to port 64h and then followed by writing data "2h" to port 60h.

If "Fast" pin is asserted, the bit 0 and 1 will reflect the status of "system reset" and "gate A20" of the emulation process when an I/O access to I/O port 60h.

I/O Port 61h(Port B)

Bit	Read/Write	Function
0	R/W	Timer 2 Gate.
1	R/W	Speaker Output Enable.
2	R/W	Parity Check Enable.
3	R/W	I/O Channel Check Enable.
4	R	Refresh Detect.
5	R	Timer OUT2 Detect.
6	R	I/O Channel Check.
7	R	System Parity Check.

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I/O Port 64h

I/O port 64h is used to emulate the register inside the keyboard controller to generate a fast reset pulse. Fast reset pulse is generated by writing data FEh to port 64h. The pulse can be generated immediately after the I/O write happens if bit 6 of Index 21h is set, otherwise it will be asserted 2 Us later.

Port 70h

Bit	Read/write	Function	Polarity
7	R/W	NMI Enable	0

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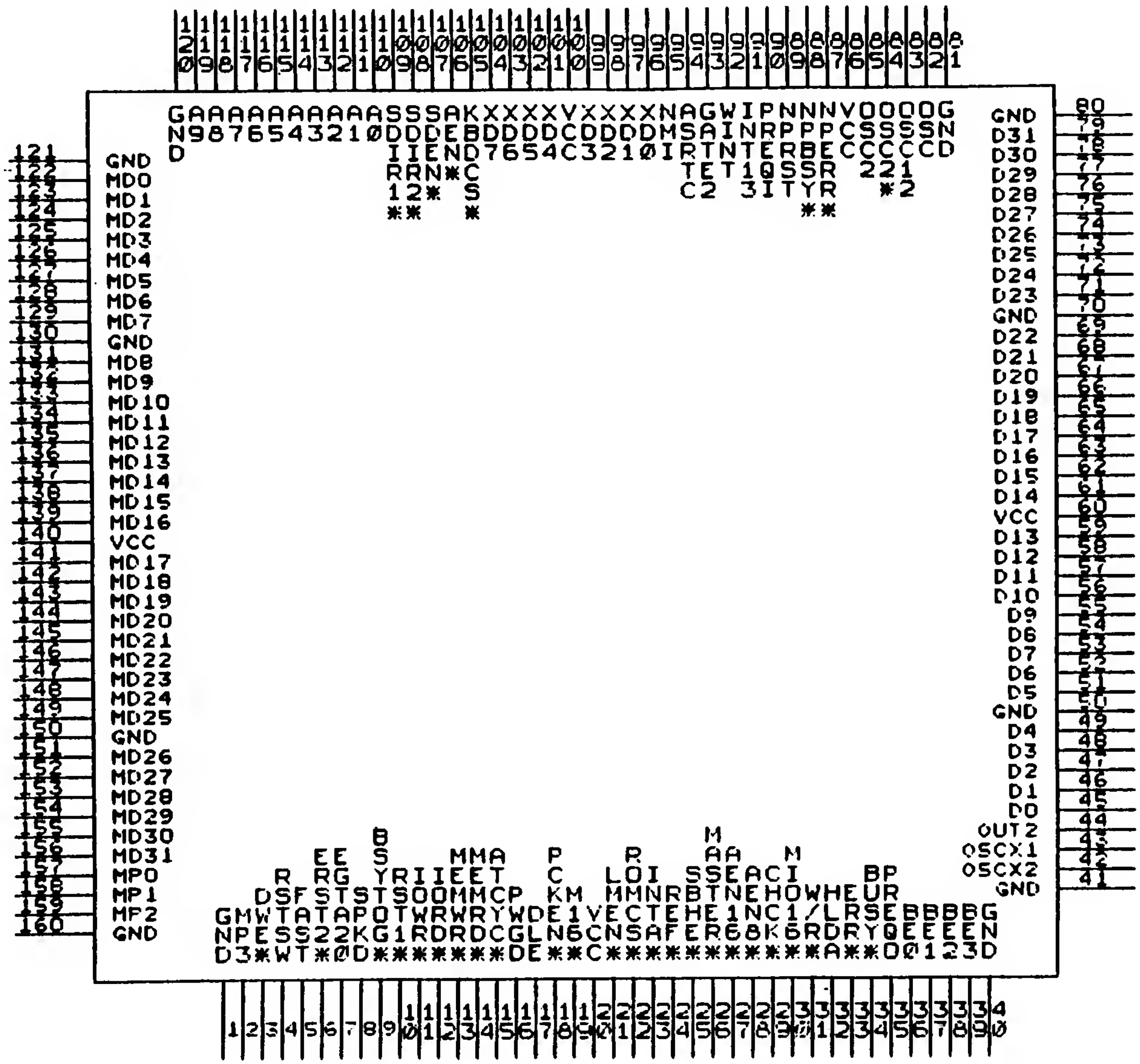
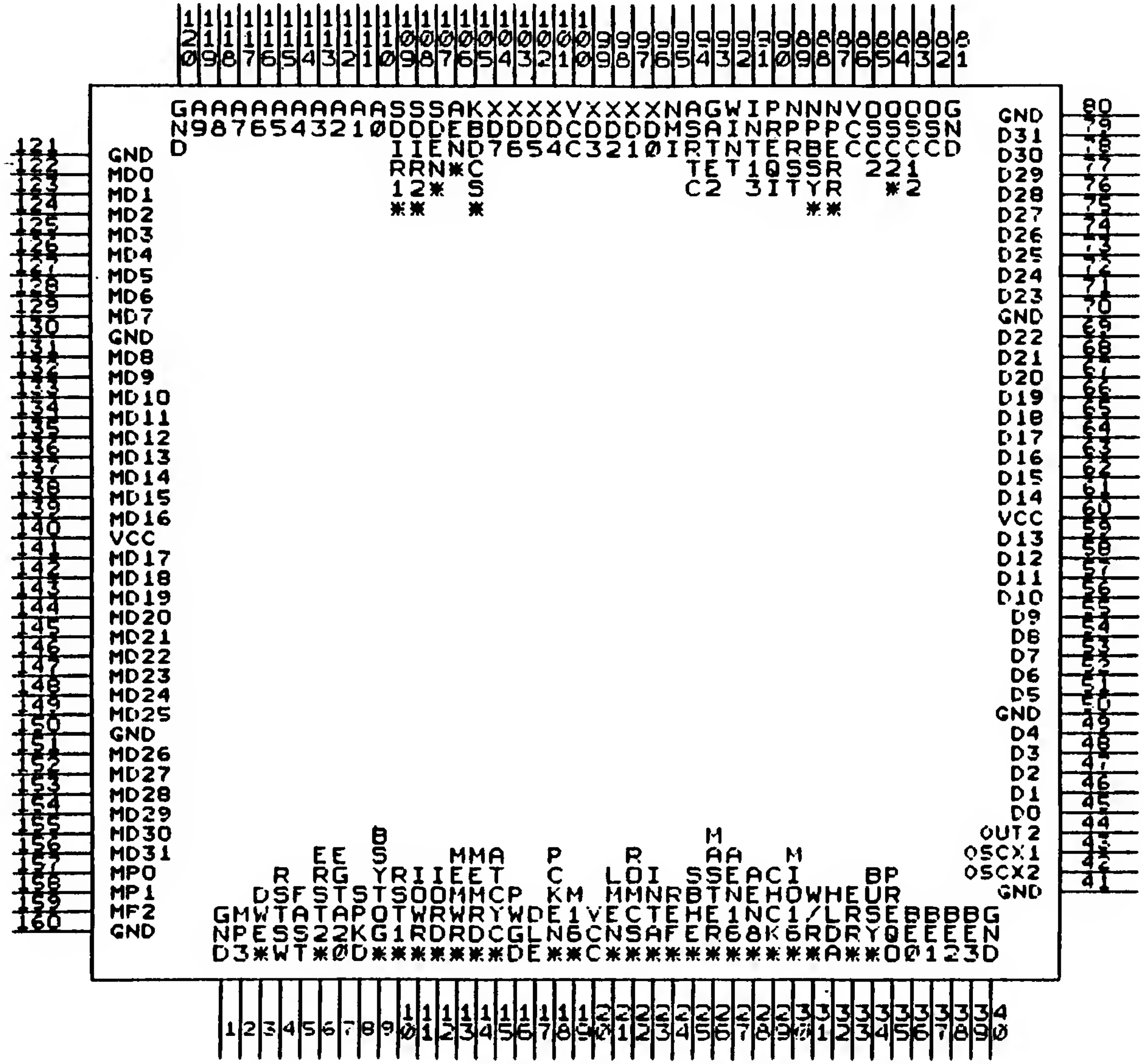


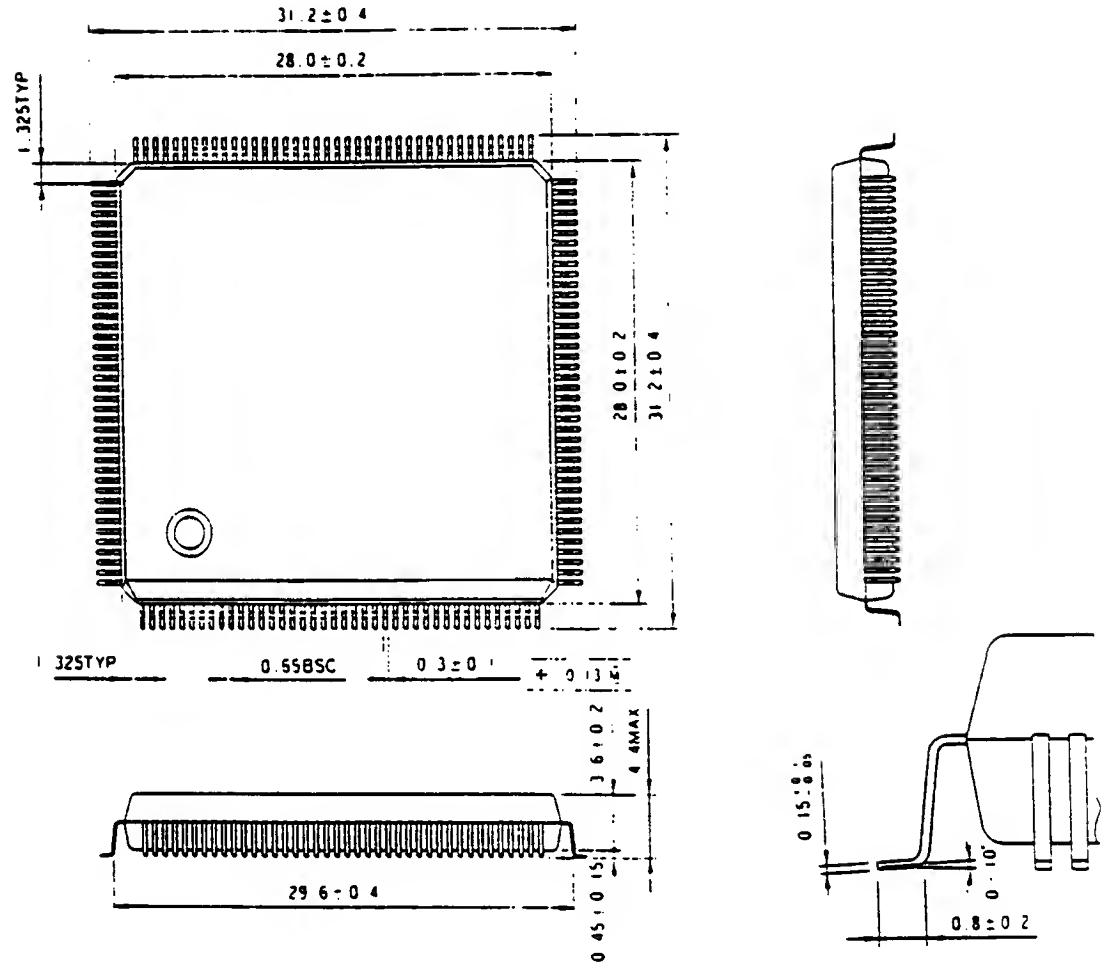
Title	
	82C392 PINOUT
Size	Document Number	REV
A		
Date: November 2, 1990	Sheet of



Title	82C392 PINOUT	
Size A	Document Number	REV
Date: November 2, 1990	Sheet of	

160-Pin Plastic Flat Package

Unit: mm



OPTi-386WB COMPATIBILITY TEST REPORT

12/19/90

VEMDER	*PRODUCT*	*VERSION*	*STATUS*
Operating Systems			
Microsoft	DOS	3.3	Pass
IBM	OS/2	1.1	Pass
IBM	OS/2	1.2	Pass
Santa Cruz Op.	SCO UNIX V		Pass
Microsoft	Windows	2.11	Pass
Microsoft	Windows	3.0	Pass
CAD/Graphics			
Autocad	Autocad	2.62	Pass
Autocad	Autocad	10	Pass
Orcad	Orcad	3.10	Pass
View Logic	Workview	4.0	Pass
Diagnostics/Demonstrations			
Diagsoft	QAPLUS	4.52	Pass
Touchstone	Checkit	2.01	Pass
IBM	Advance Diagnostics	2.01	Pass
DataBase Group	Power Meter	1.2, 1.5	Pass
Landmark	Landmark	1.14	Pass
PC Labs	Benchmark	4.2	Pass
BrownBag Softw	Ramtest	2.00, 3.00	Pass
Network/Communication			
Novell	Netware 386 Server/Station	3.1	Pass
Hayes	Smartcom II		Pass
Utilities			
Norton	Norton Uilities	4.5	Pass
Central Point	PCTOOLS	5.5	Pass
Executive Sys.	Xtree-Pro	1.0	Pass

EMS Emulators

Quarterdeck	QEMM	5.0	Pass
Larson Comput.	LIM386	4.05	Pass
AMI	SEEMS	1.16	Pass

Data Base

Borland	Paradox 386	2.0	Pass

Spread Sheets

Lotus	Lotus 123	2.2	Pass
Lotus	123 w/ coprocessor	2.2	Pass
Microsoft	EXCEL	2.1p	Pass

Game/Education

Microsoft	Flight Simulator	3.0, 4.0	Pass
	DugDigger		Pass

Word Processing

Microsoft	Word	5.0	Pass
Microsoft	Pagemaker	3.0	Pass

OPTi COMPATIBILITY TEST
HARDWARE USAGE

VENDER	*PRODUCT*	*STATUS*
Disk Controller/Drive		
Adaptec	SCSI Controller AHA-1542B	Pass
NCL	SCSI Controller NCL500	Pass
Future Domain	SCSI Controller TMC-950	Pass
Adaptec	ESDI Controller ACB-2322D	Pass
Western Digi.	ESDI WD1007A-WA2	Pass
NCL	ESDI NDC535	Pass
Ultrastor Corp	ESDI Ultra/2(F) Rev D	Pass
TMC	IDE IFSP-1.00	Pass
TMC	IDE CCAT-200	Pass
Adaptec	RLL ACB-2370/72C	Pass
Seagate	RLL 8 Bit Card	Pass
Western Digi.	MFM WD1003-WA2	Pass
Western Digi.	MFM WD1006V-MM2	Pass
DTC	MFM 7280,5280	Pass

*The above Disk Controller cards are tested with the following disk drives

Maxtor	SCSI XT-4170S	Pass
Seagate	SCSI ST-125N	Pass
Fujitsu	SCSI M2611SA	Pass
Micropolis	ESDI 1355	Pass
NEC	ESDI D5655	Pass
Miniscripe	IDE 8051A	Pass
Corner	IDE CP3104	Pass
Toshiba	RLL MK134FA	Pass
Seagate	MFM ST-Series	Pass

VENDER	PRODUCT	STATUS
Video Card		
Orchid	Pro-Designer, Tseng-Labs chip 8 Bit VEGA	Pass
Orchid	Pro-Designer, Tseng-Labs chip 16 Bit VGA	Pass
Orchid	Pro-Designer II, Tseng-Labs Chip 16 Bit VGA	Pass
ATI	Wonder-16 16 Bit VEGA	Pass
LCS	LCS-8856 Cirrus Logic 8 Bit VEGA	Pass
VIDEO-7	V-RAM VGA	Pass
Paradise	VGA-Plus W.D. 16 Bit VGA	Pass
Infiniti	INVGA W.D. 16 Bit VGA	Pass
Coprocessor		
Intel	80387	Pass
Cyrix	83D87	Pass
Weitek	3167	Pass
Memory Card		
Intel	Above Board	Pass
Everex	RAM-10000	Pass
Mouse		
PC Mouse	Serial Interface	Pass
Logitech	Serial/Bus	Pass

OPTi-386WB TMP Board
12/19/90

(I) Jumper Settings

(a) Cache

	JP5	JP6	JP7	JP8	JP9	JP10
32K	1-2	1-2	1-2	Open	2-3	2-3
64K	2-3	1-2	1-2	Open	2-3	1-2
128K	2-3	1-2	2-3	Close	2-3	1-2
256K	2-3	2-3	2-3	Close	1-2	1-2

Notes:

- Cache even bank: U34, U35, U36, U37
  Cache odd bank: U43, U44, U45, U46
  Tag RAM: U32, U33, U42
- 32K cache, put 8Kx8 SRAM at even bank,
  4Kx4 SRAM at U32 and U33, 16Kx1 SRAM at U42
- 64K cache, put 8Kx8 SRAM at both even & odd bank,
  4Kx4 SRAM at U32 and U33, 16Kx1 SRAM at U42
- 128K cache, put 32Kx8 SRAM at even bank
  16Kx4 SRAM at U32 and U33, 16Kx1 SRAM at U42
- 256K cache, put 32Kx8 SRAM at both even & odd bank,
  4Kx4 SRAM at U32 and U33, 16Kx1 SRAM at U42

(b) JP1: OPEN color monitor
CLOSE monochron monitor

(c) JP2: 2-3 normal operation
1-2 clear CMOS memory

(d) JP3: OPEN - AT Bus clock is CPU clock divided by 6
CLOSE - AT Bus clock is CPU clock divided by 8

(II) SRAM/DRAM Speed

	Cache SRAM	Tag SRAM	DRAM*
33MHz	25ns	15ns	80ns
40MHz	20ns	15ns	80ns

* DRAM at minimum wait state

OPTi-386WB Schematic Change History
12/19/90

386WB schematic Rev.A dated 12/18/90 is the latest and greatest. Customers who have Rev.1 schematic dated 11/16/90, please see Part I for changes. Customers who have Rev.1 schematic dated 9/28/90, please see Part II for changes.

On the Bill of Materials Rev.A dated 12/18/90, item 9 is test pins which is for debugging prupose, they are not needed for production boards.

Part I:

The following changes have been implimented at the Rev.A 386WB schematic dated 12/18/90, from Rev.1 schematic dated 11/26/90.

(1) Battery circuit has been changed to suit for rechargeable battery, on schematic sheet 7

(2) RA1 and RA2 have been changed, was 75 OHM, is 33 OHM on schematic sheet 10

(3) Add eight 15pf capacitors C122-C129 to CAS lines, on schematic sheet 10

Part II:

The following changes have been implimented at the Rev.A 386WB schematic dated 12/18/90, from Rev.1 schematic dated 9/28/90.

(1) Battery circuit has been changed to suit for rechargeable battery, on schematic sheet 7

(2) RA1 and RA2 have been changed, was 75 OHM, is 33 OHM on schematic sheet 10

(3) Add eight 15pf capacitors C122-C129 to CAS lines, on schematic sheet 10

(4) LA(23:17) pull up resistor pak RP7, was 10K, is 2.2K on schematic sheet 5

(5) CPU clock generation circuit damping resistors around the oscillator, on schematic sheet 4
R28 was 27 OHM, is 10 OHM
R22, R27, R30, R31 was 27 OHM, is 22 OHM

(6) Add a 33 OHM resistor R29 on RFSH# signal, on schematic sheet 4 lower right corner

OPTi-386WB Benchmark Test Report
12/19/90

Configuration: 386WB TMP Board, 64K Cache, 8M DRAM on board

Power Meter 1.5:	33MHz - 8.293 mips
	40MHz - 9.968 mips

Landmark 1.14:	33MHz - 54.8 mhz
	40MHz - 65.7 mhz

PC Magazine 5.5:

33MHz -	CPU instruction mix	1.59 seconds
	CPU 128 NOP loop	1.00 seconds
	CPU do nothing loop	0.77 seconds
	CPU integer addition	0.37 seconds
	CPU integer multiple	0.25 seconds
	CPU string sort & move	0.49 seconds
	CPU prime number sieve	0.24 seconds
	CPU floating point mix	2.86 seconds
	Convention memory read	0.28 seconds
	Convention memory write	0.22 seconds
	Extended memory read	0.88 seconds
	Extended memory write	0.82 seconds
40MHz -	CPU instruction mix	1.33 seconds
	CPU 128 NOP loop	0.82 seconds
	CPU do nothing loop	0.64 seconds
	CPU integer addition	0.31 seconds
	CPU integer multiple	0.20 seconds
	CPU string sort & move	0.40 seconds
	CPU prime number sieve	0.20 seconds
	CPU floating point mix	2.42 seconds
	Convention memory read	0.22 seconds
	Convention memory write	0.22 seconds
	Extended memory read	0.71 seconds
	Extended memory write	0.65 seconds

Norton SI 4.5, Computing Index:	33MHz - 43.2
	40MHz - 48.3

Byte Magazine 1.3, CPU Index:	33MHz - 6.54
	40MHz - 7.82

Item	Quantity	Reference	Part
1	2	J11,J12	PS CON
2	64	C31,C18,C25,C26,C27,C37, C38,C39,C40,C41,C42,C43, C44,C45,C46,C47,C55,C56, C57,C58,C59,C61,C62,C63, C64,C66,C67,C68,C70,C71, C72,C73,C78,C81,C82,C83, C84,C85,C87,C88,C91,C93, C94,C96,C97,C98,C99,C100, C101,C102,C103,C104,C107, C108,C109,C110,C111,C112, C113,C114,C116,C117,C118, C119	0.1UF
3	40	C6,C1,C2,C3,C4,C5,C7,C8, C9,C10,C11,C12,C13,C14, C15,C16,C21,C22,C23,C24, C32,C33,C34,C35,C36,C48, C49,C50,C51,C52,C53,C54, C74,C75,C79,C80,C95,C105, C106,C115	10UF TANT
4	3	C60,C59A,C77	0.001UF
5	2	C65,C69	1.0UF
6	1	U17	80386
7	11	RP11,RP1,RP5,RP8,RP10, RP12,RP13,RP14,RP18,RP20, RP21	RSIP9 10K
8	1	U16	3167/387
9	12	5,1,2,3,4,6,7,8,9,10,11, 12	TEST PIN
10	1	R19	510
11	3	U33,U32,U42	16KX4 W/O
12	3	JP8,JP1,JP3	JUMPER
13	2	U41,U8	74LS244
14	6	JP7,JP2,JP5,JP6,JP9,JP10	3-W JUMP
15	8	U37,U34,U35,U36,U43,U44, U45,U46	8KX8/32KX8
16	4	RA11,RA9,RA10,R32	27

Item	Quantity	Reference	Part
17	2	RP15,RP19	RSIP9 4.7K
18	2	RP17,RP16	RSIP7 4.7K
19	2	U29,U26	74F08
20	1	U28	74F86
21	6	RP22,RP2,RP3,RP4,RP6,RP9	RSIP7 10K
22	3	U30,U9,U10	74ALS245
23	1	U14	27512
24	1	SW2	ON-OFF SW
25	2	C120,C29	10UF
26	1	U27	66MHZ
27	1	U31	SYSC
28	11	C86,C90,C92,C122,C123, C124,C125,C126,C127,C128, C129	15PF
29	10	D10,D3,D4,D5,D6,D7,D8,D9, D11,D12	1N4146
30	1	U5	74LS14
31	1	L5	INDUCTOR
32	8	R26,RA1,RA2,R14,R15,R25, R29,R34	33
33	12	R22,RA3,RA4,RA5,RA6,RA7, RA8,R23,R24,R27,R30,R31	22
34	2	R28,R20	10
35	1	Y2	14.3MHZ
36	1	U15	DBC
37	1	J24	CON-4
38	1	SW1	SW PUSHBUTTON
39	1	C121	TANT 10UF
40	1	R21	1M

Item	Quantity	Reference	Part
41	3	C89,C30,C76	22PF
42	1	D13	1N917
43	1	JP4	TURBO LED
44	5	U7,U4,U11,U12,U13	74LS245
45	1	U2	74F125
46	3	R10,R11,R13	1K
47	2	R35,R6	51
48	1	RP7	RSIP7 2.2K
49	9	J21,J2,J3,J4,J5,J6,J7,J8, J9	CON-31X2
50	9	J22,J13,J14,J15,J16,J17, J18,J19,J20	CON-18X2
51	1	Q2	2N3906
52	1	Q1	2N3904
53	1	U1	8042
54	1	U6	82C206
55	1	Y1	32.8K
56	1	C28	0.0047UF
57	2	C19,C20	47PF
58	1	C17	470PF
59	2	D1,D2	1N4148
60	1	R12	2M
61	2	R9,R7	10K
62	1	R8	51K
63	1	F1	FUSE
64	4	L1,L2,L3,L4	FB
65	1	U3	MC14069
66	2	R3,R5	2K

Item	Quantity	Reference	Part

67	5	R4,R2,R16,R17,R18	330
68	1	R33	150
69	1	R36	100
70	2	D14,D15	1N914
71	1	J19	EXT BATCON
72	1	BT1	3.6V
73	1	J23	KEYLOCK CON
74	1	J1	KEYBRD CON
75	1	R1	4.7K
76	3	U38,U39,U40	74F244
77	8	U25,U18,U19,U20,U21,U22, U23,U24	SIMM

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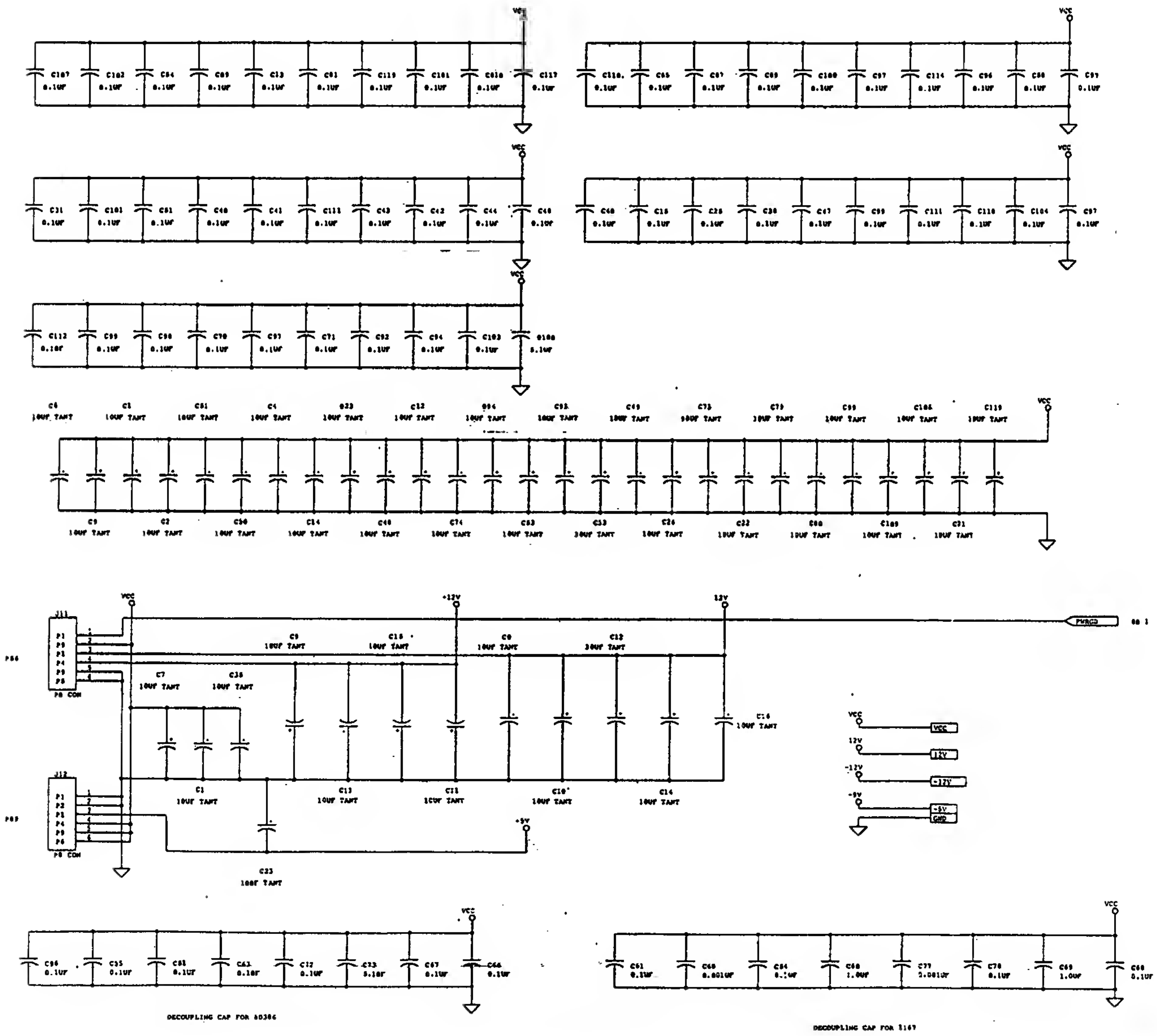
NOTE:

1. ALL CAPS ARE 25V AND IN UF UNLESS OTHERWISE SPECIFIED.
2. ALL RESISTORS ARE 1/4W AND IN OHM UNLESS OTHERWISE SPECIFIED



49

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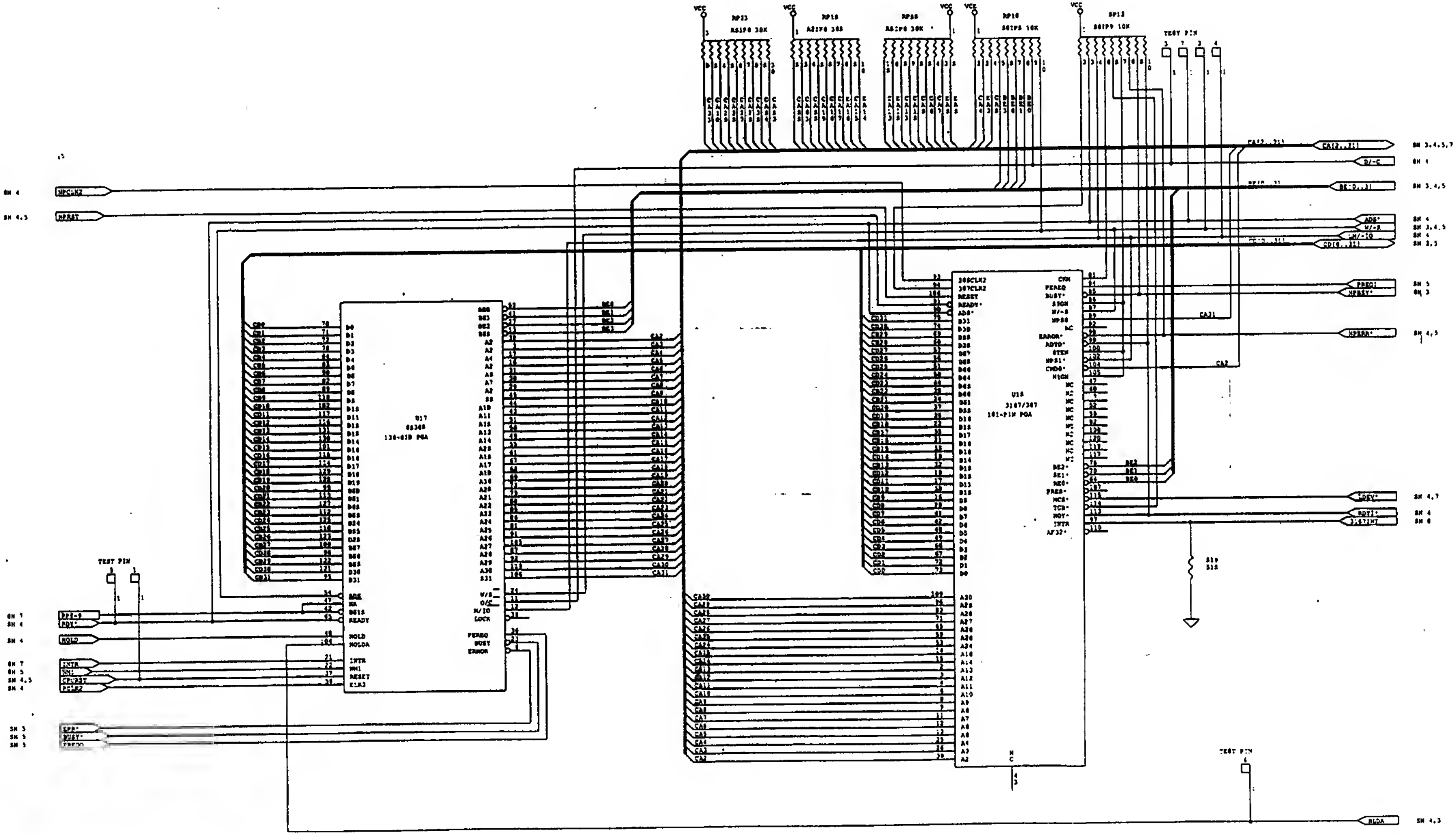

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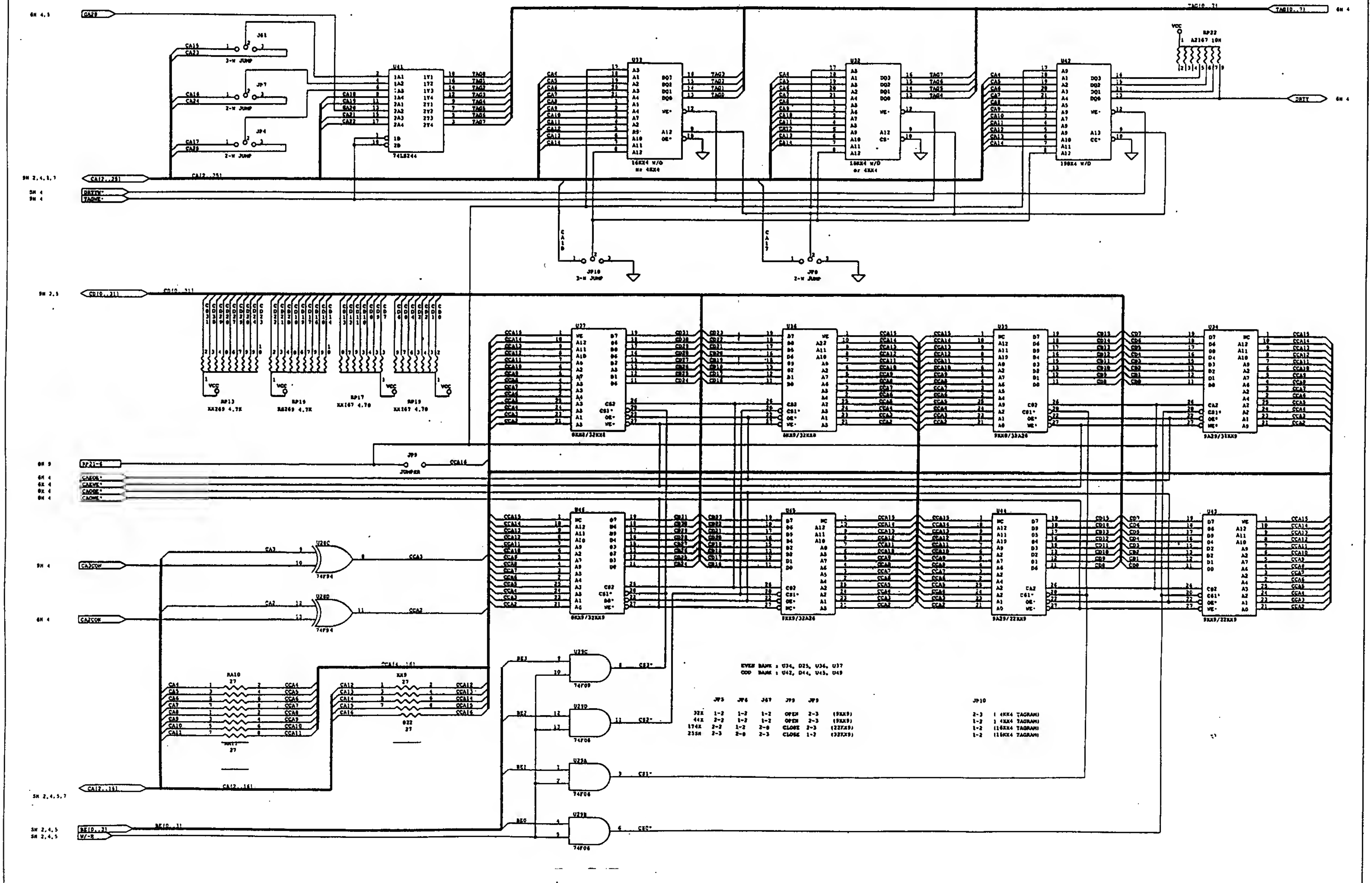

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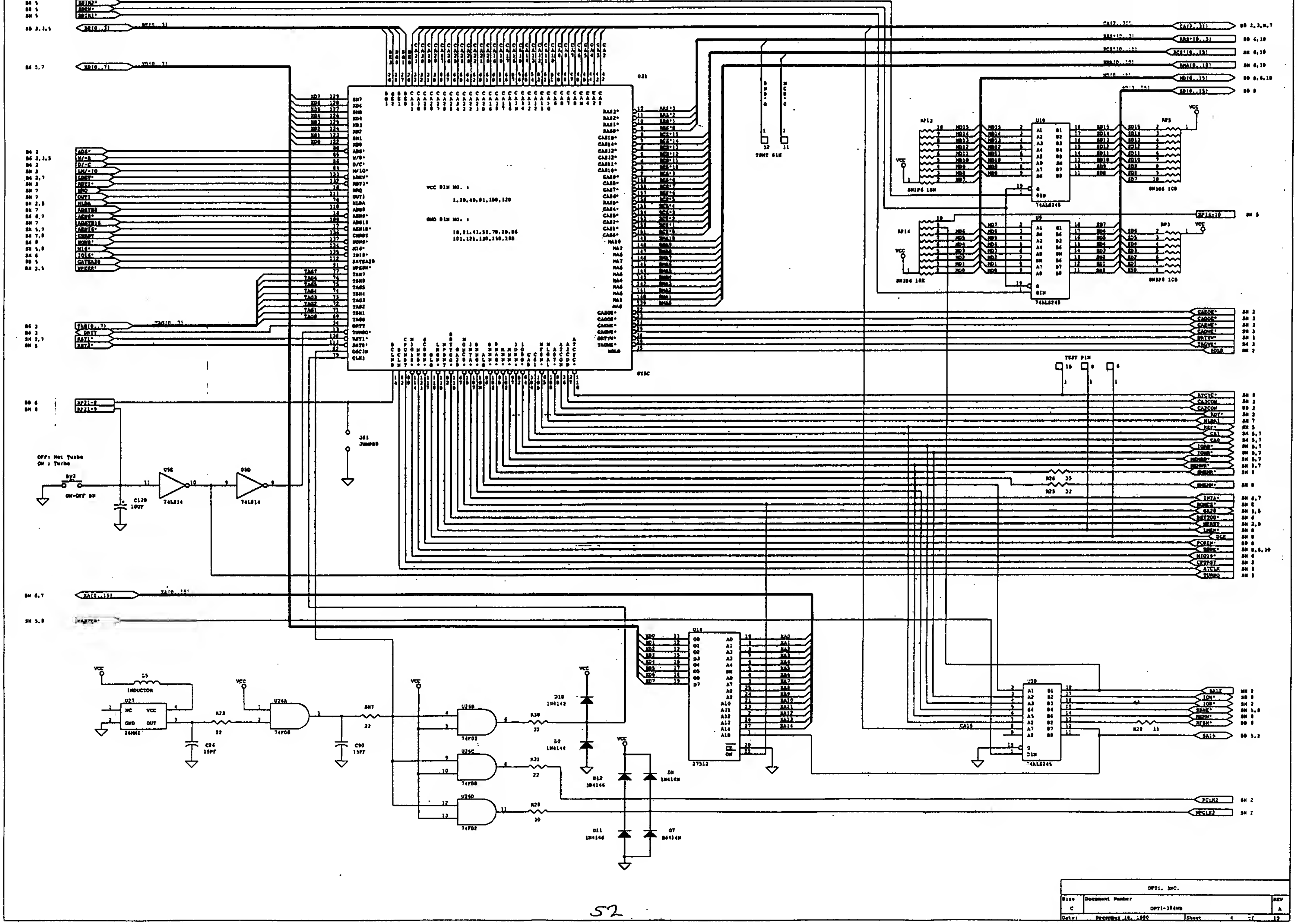
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Size C
Document Number OPTi-386WB
REV A
Date: December 18, 1990
Sheet 4 of 12
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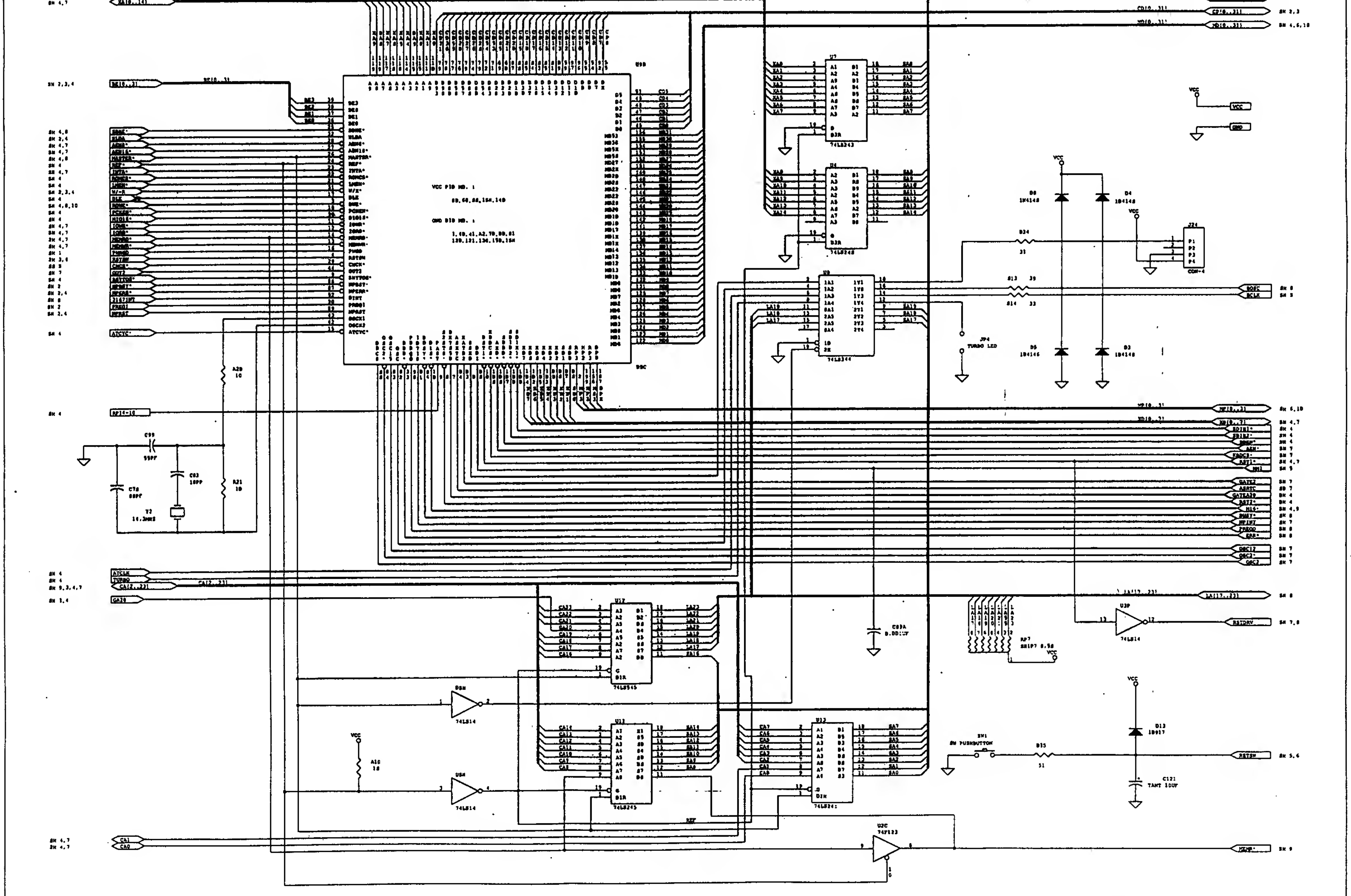
ON : Turbo
ON-OFF SW
INDUCTOR
TEST PIN
JUMPER



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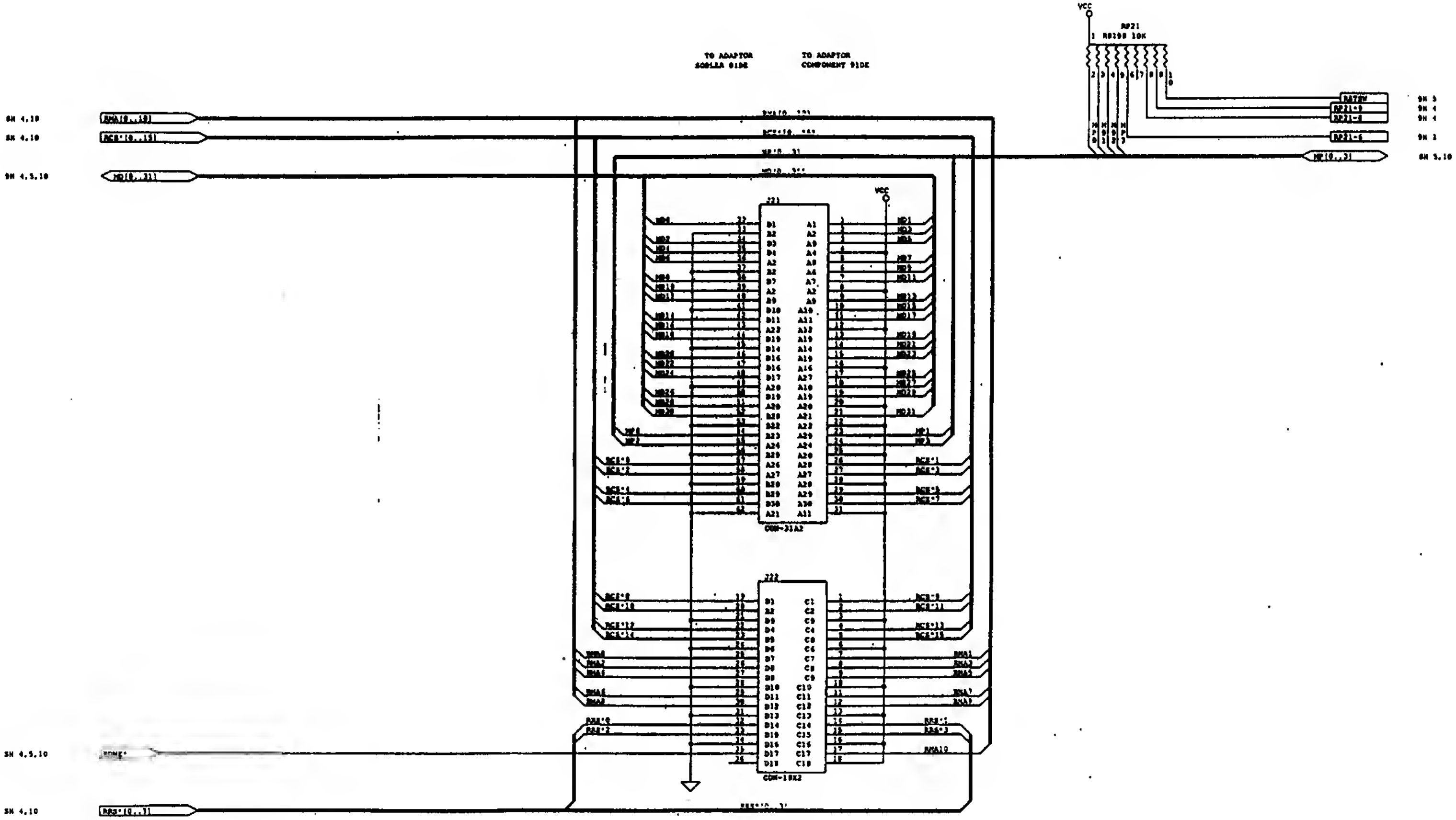
Size C	Document Number OPTI-386WB	REV A
Date: December 18, 1992	Sheet 5 of	

53



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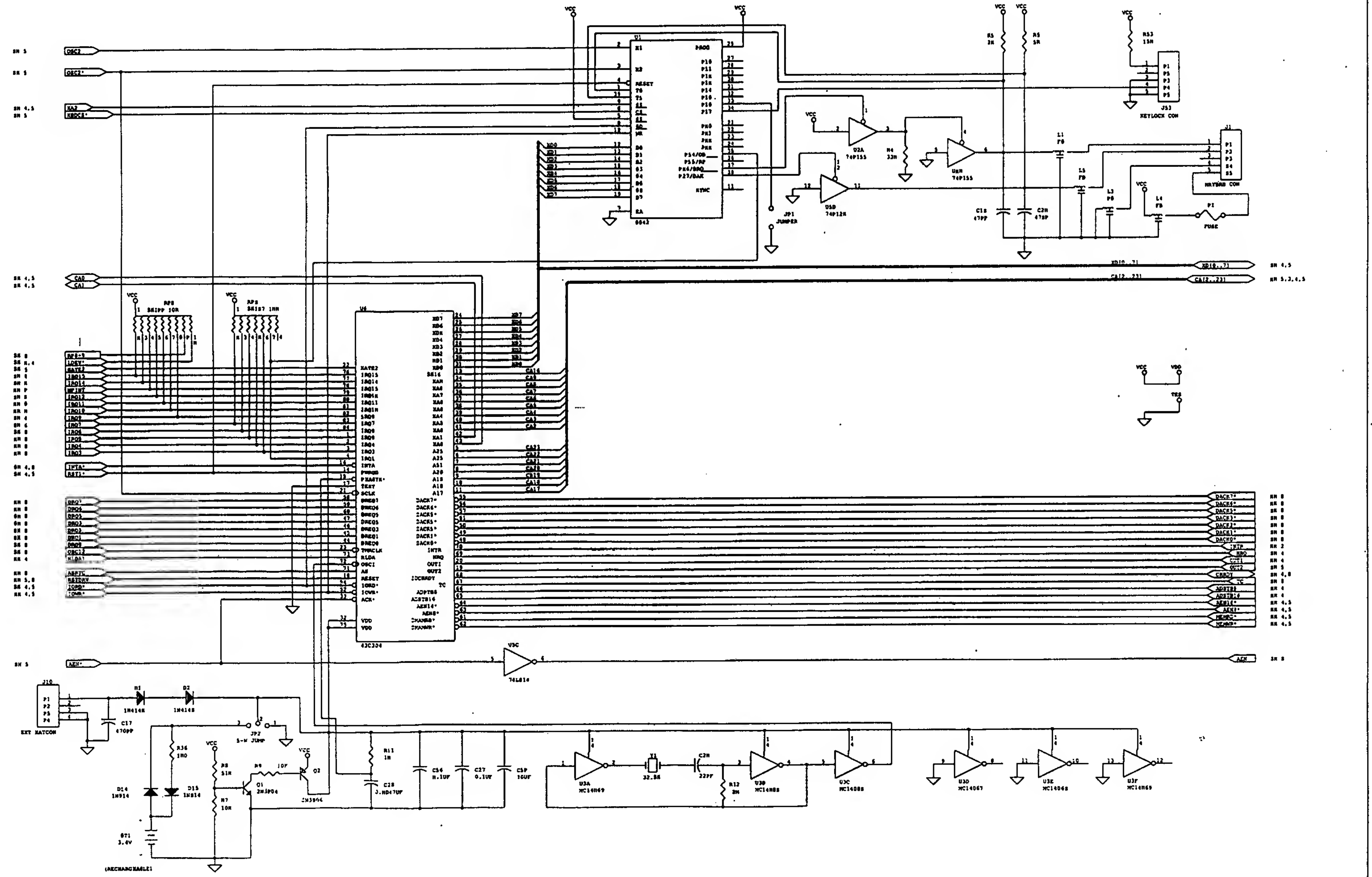
54



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Size C | Document Number OPTi-386WB | REV A

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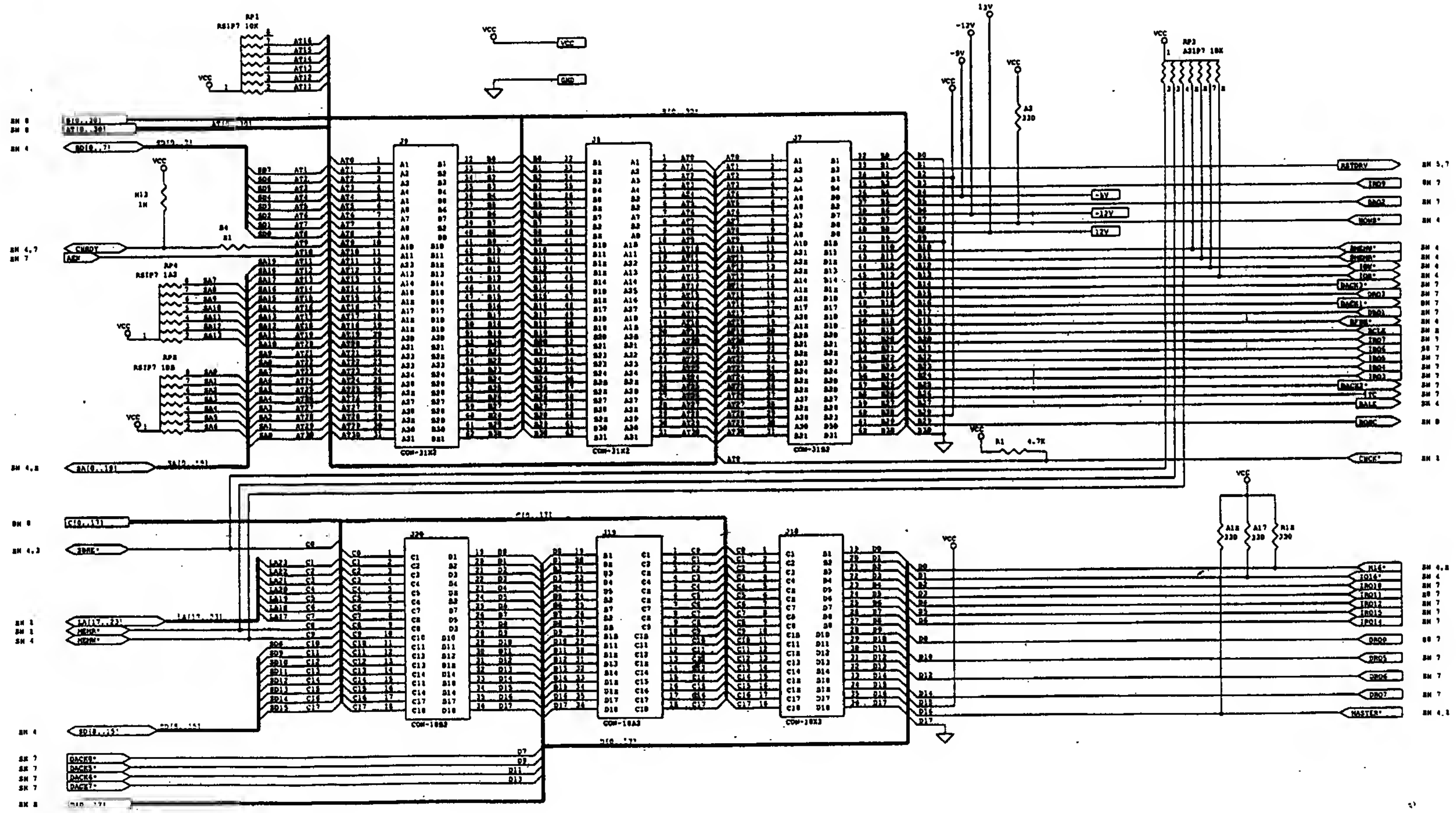

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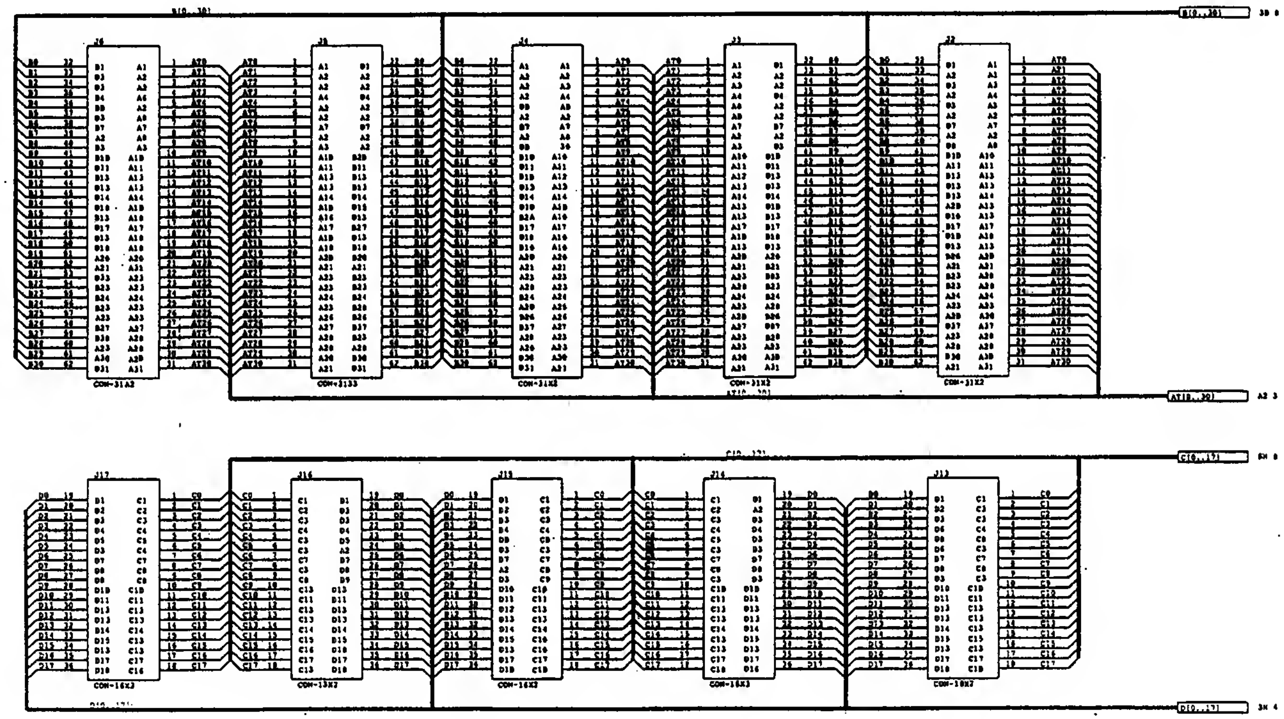

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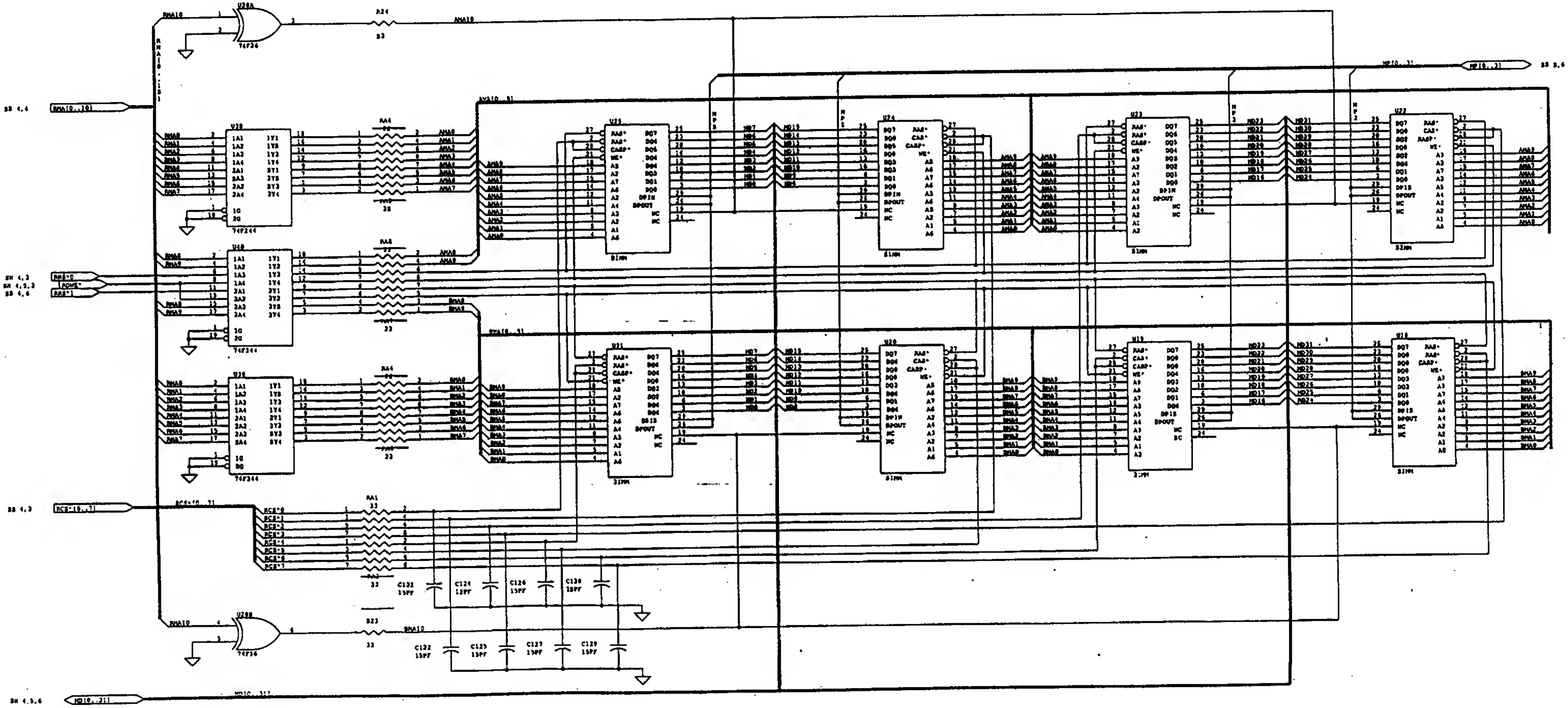

58

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